11/15/00

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JC921 U.S. PTO 11/14/00

PTO/SB/05 (08-00)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	COLGRA P21AUS
First Inventor	Robin HARKER
Title	COMPUTER SYSTEMS
Express Mail Label No.	EL469354180US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. [X] Applicant claims small entity status. See 37 CFR 1.27.
3. [X] Specification [*Total Pages* 8]
(preferred arrangement set forth below)
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 4]
5. Oath or Declaration [*Total Pages* 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63 (d)) *(for continuation/divisional with Box 17 completed)*
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. [ ] Application Data Sheet. See 37 CFR 1.76
7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] paper
   c. [ ] Statements verifying identity of above copies

JC825 U.S. PTO 09/711983 11/14/00

ACCOMPANYING APPLICATION PARTS

9. [ ] Assignment Papers (cover sheet & document(s))
10. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [X] Other: Express Mail Certificate

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No.: _____ / _____

Prior application information. Examiner _____ Group / Art Unit. _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

PATENT & TRADEMARK OFFICE

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or [ ] *Correspondence address below*

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City		*State*		*Zip Code*	
Country		*Telephone*		*Fax*	

Name (Print/Type)	Michael J. Bujold	*Registration No. (Attorney/Agent)*	32,018
Signature	Michael Bujold	*Date*	11/14/00

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11/14/00 PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Robin HARKER
Serial no.	:	
Filed	:	
For	:	COMPUTER SYSTEMS
Group Art Unit	:	
Examiner	:	
Docket	:	COLGRA P21AUS

The Commissioner of Patents and Trademarks
Washington, D.C. 20231

EXPRESS MAIL CERTIFICATE

"Express Mail" label number: **EL469354180US**
Date of Deposit: **11/14/00**

I hereby state that the following attached paper or fee:

Patent Application Transmittal-1 pg.;
Fee Transmittal Ltr (+Dupl)-1 pg.;
Check for $355;
Specification/Claims/Abstract- 8 pgs.;
Drawings - 4 pgs.;
Declaration & Power of Atty- 2 pgs.;
Return Postcard

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR § 1.10, on the date indicated above and is addressed to the Assistant Commissioner of Patents, Washington, D.C. 20231.

Michael J. Bujold

Signature of person mailing paper or fee

NOTE: *The label number need not be placed on each page. It should, however, be placed on the first page of each separate document, such as, a new application, amendment, assignment, and transmittal letter for a fee, along with the certificate of mailing by "Express Mail." Although the label number may be on checks, such a practice is not required. In order not to deface formal drawings, it is suggested that the label number be placed on the back of each formal drawing or the drawings be accompanied by a set of informal drawings on which the label number is placed.*

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FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 355

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Robin HARKER
Examiner Name	
Group Art Unit	
Attorney Docket No.	COLGRA P21AUS

METHOD OF PAYMENT

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 04-0213

Deposit Account Name: DAVIS AND BUJOLD

[X] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

[X] Applicant claims small entity status. See 37 CFR 1.27

2. [X] **Payment Enclosed:**

[X] Check [ ] Credit card [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	355
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 355

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below	Fee Paid
Total Claims	12	-20** = 0	X	0	= 0
Independent Claims	1	- 3** = 0	X	0	= 0
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) -0-

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) -0-

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Michael J. Bujold	Registration No. (Attorney/Agent)	32,018	Telephone	603-624-9220
Signature	Michael Bujold			Date	11/14/00

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Computer Systems

This invention relates to computer systems, and is concerned especially with computer systems of the kind that involve the interconnection or clustering of a multiplicity of processors.

Background of the Invention

It is known to form a computing system of the above-specified kind by interconnecting the processing units of a multiplicity of personal computers (PCs) and operating them in parallel with one another; such systems are sometimes referred to as 'Beowulf clusters'. The central processing units (CPUs) of Pcs provide significant computing power at relatively-low cost, and advantage has been taken of this to form systems of the above-specified kind having very high computing power comparable with that of a specially-designed supercomputer, at a fraction of the supercomputer-cost. In such systems a multiplicity of PC-CPUs are interconnected and operated in parallel with one another as separate nodes of a local area network. These systems using clustered CPUs require the development of special software to enable parallel operation, and are generally slower than their supercomputer counterparts, but have significant advantage economically.

The CPUs of Pcs are not designed to have the extended reliability to be expected of a supercomputer, so computing systems of the known form involving clustered CPUs are, in comparison, susceptible to faults. A fault occurring in an individual CPU will disrupt processing of the current application, and although the application can in general be re-started without replacement of the faulty unit, the disruption and loss of computing time involved is undesirable.

It is one of the objects of the present invention to provided a computer system of the said above-specified kind, which whilst having the potential for cost advantage of the known clustered PC-CPU systems, is less susceptible to fault disruption.

Summary of the Invention

According to one aspect of the present invention there is provided a computer system of the said above-specified kind wherein power supply to each processor is from a common power-supply means having fault-tolerating redundancy.

The computer system of the present invention may, especially for cost-advantage, utilise processors that are a form such as used in the context of PC computers. However, in accordance with the present invention, rather than powering each processor from its own power-supply unit as in the case of the known form of computer system referred to above utilising PC-CPUs, they are powered from common power-supply means. The power-supply units of PC-CPUs especially, are not designed to have long fault-free operation so the likelihood of a fault arising in any of a multiplicity of clustered PC-CPUs, can be significantly high. The individual power-supply units might be replaced by units with a higher standard of reliability, but it is generally more economical to provide a common power-supply means and invest this with an even higher standard of reliability and, moreover, to include fault-tolerating redundancy within it.

The processors of the computer system according to the invention may be carried by individual printed-circuit boards, for example PC motherboards, that are mounted together side-by-side within a rack-mounting. The rack-mounting may be contained within a cabinet together with the power-supply means.

The power-supply means may involve one or more power-supply units each of which comprises a plurality of power-supply modules which operate in parallel with one another in supplying power to the processors. The modules may each include diode or other circuitry that is responsive to the occurrence of a fault within the module (eg reduction in its voltage output in relation to that of the other module) to isolate that module effectively from the processors. Where more than one power-supply unit is involved, they may act in parallel with one another to power all the processors together.

Brief Description of the Drawings

A computer system in accordance with the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a front elevation of the computer system according to the invention, with the front panel of the cabinet housing the system removed;

Figure 2 is a sectional plan of the computer system of Figure 1 showing only two of its five processing modules with one fully inserted and the other only partially inserted;

Figure 3 is a sectional side elevation of the computer system of Figure 1; and

Figure 4 is a schematic representation of the power distribution circuitry of the computer system of Figure 1.

Description of the Preferred Embodiments

Referring to Figures 1 to 3, the computer system of the invention is housed within a standard computer cabinet 1 which contains racking (not shown in detail) for

supporting five processor modules 2 side-by-side within the cabinet 1. Each processor module 2 includes an L-shape plate 3 (see Figure 3) by which it is supported in the cabinet 1, the plate 3 being held upright by engagement of its top and bottom edges 4 and 5 within grooved tracks 6 and 7, respectively, of the racking, so that the module 2 can be readily slid in and out of the cabinet 1 on the tracks 6 and 7. Handles 8 are provided at the front of each module 2 to assist with insertion and withdrawal, and power connection to the module 2 is established when the module 2 is fully inserted, via a two-part plug-and-socket connector 9 (shown as a single block) at the rear of the projecting base-part 10 of the L-shape plate 3.

Each plate 3 carries a PC-CPU motherboard 11 that is mounted in spaced face-to-face relationship with it immediately behind a front-panel 12 of the module 2. This enables data connections to be readily made with its processor 13 and a plug-in network card 14 (see Figure 3) and other circuitry (not shown) of the motherboard 11, via connectors 15 on the front-panel 12. The motherboard 11 is interconnected by wiring (not shown) for data interchange with a hard-disk unit 16 mounted on the projecting base-part 10 of the plate 3, and is powered along with the unit 16 by connections (not shown) from the connector 9.

Referring also now to Figure 4, power is supplied to all five processor modules 2 in parallel via a wiring loom 17 which interconnects their connectors 9 with two power-supply units 18. The units 18, which are mounted at the back of the cabinet 1 to lie above the base-parts 10 of the five plates 3, each comprise two, redundant power-supply modules 19. The two modules 19 supply power in parallel with one another, and each includes diode circuitry 20 (indicated in Figure 4 in the case of one

module 19 only). The circuitry 20 is operative to isolate the respective module 19 from its paired module 19 and the loom 17 generally, in the event that a fault occurs by which the voltage output of the module 19 falls so that current would otherwise flow to it rather than from it.

The two units 18 operate in parallel with one another in supplying power to the five processor modules 2, so that the operation in parallel of the four power-supply modules 19 is with a significant degree of redundancy for power-supply fault-survival.

The five processor modules 2 are interconnected via the connectors 15 and network cards 14 by data-cabling (not shown) to operate in parallel with one another as individual nodes of a local-area network and provide a high-powered computing capability. The PC motherboards 11 used, have a high degree of reliability, and that same degree of reliability is afforded to the computer system as a whole by the use of the highly-reliable form of powering adopted.

Although in the above example the modules 2 are operated in parallel, this need not be the case where, for example, a high processor density is required. A high processor density is required for example by internet service providers, when establishing a large number of web servers.

Claims:

1. A computer system comprising a multiplicity of processors interconnected with one another, and power-supply means common to all said processors, wherein said power-supply means includes means affording fault-tolerating redundancy.

2. A computer system according to Claim 1 wherein the processors are interconnected for operation in parallel with one another.

3. A computer system according to Claim 1 comprising a multiplicity of processor modules, said processors being carried by the processor modules respectively, cabinet means, means mounting the processor modules side-by-side with one another within said cabinet means, and means mounting the power-supply means within the cabinet means.

4. A computer system according to Claim 3 wherein the means mounting the processor modules within the cabinet means comprises racking, the racking includes tracks, and the processor modules are mounted on said tracks for sliding movement selectively in and out of said cabinet means.

5. A computer system according to Claim 1 wherein the power-supply means comprises a plurality of power-supply modules, and means coupling the power-supply modules in parallel with one another for supplying power to the processors.

6. A computer system according to Claim 5 wherein each power-supply module includes circuitry responsive to the

occurrence of a fault within that respective power-supply module to isolate that individual power-supply module from supplying power to the processors.

7. A computer system according to Claim 6 wherein said circuitry is diode circuitry.

8. A computer system according to Claim 6 wherein said circuitry of each power-supply module is responsive to reduction in voltage output of the respective power-supply module to isolate that individual power-supply module from supplying power to the processors.

9. A computer system according to Claim 1 wherein the power-supply means comprises a plurality of pairs of power-supply modules, means coupling the two power-supply modules of each said pair together for supplying power in parallel with one another, and means coupling the pairs of power-supply modules in parallel with one another for supplying power to the processors.

10. A computer system according to Claim 9 wherein each power-supply module of each pair includes circuitry responsive to the occurrence of a fault within that respective power-supply module to isolate that power-supply module from supplying power in parallel with the other power-supply module of the respective pair.

11. A computer system according to Claim 10 wherein said circuitry is diode circuitry.

12. A computer system according to Claim 10 wherein said circuitry of each power-supply module is responsive to reduction in voltage output of the respective power-supply module to isolate that individual power-supply module from supplying power to the processors.

Abstract:

Computer Systems

Processor modules 2 are supported side-by-side with one another to slide in and out of a cabinet 1 on tracks 6,7, each module 2 including a PC-CPU motherboard 11 and a hard-disk unit 16 mounted on a metal plate 3. Power is supplied to all the modules 2 in parallel from two power-supply units 18 mounted in the back of the cabinet 1, each comprising a pair of power-supply modules 19. The pairs of power-supply modules 19 supply power in parallel with one another to the processor modules 2. Diode circuitry 20 is included in each power-supply module 2 to isolate that power-supply module 2 from its paired power-supply module 2 in the event that a fault occurs by which the output voltage of the respective power-supply module 2 falls below that of the power-supply module with which it is paired.

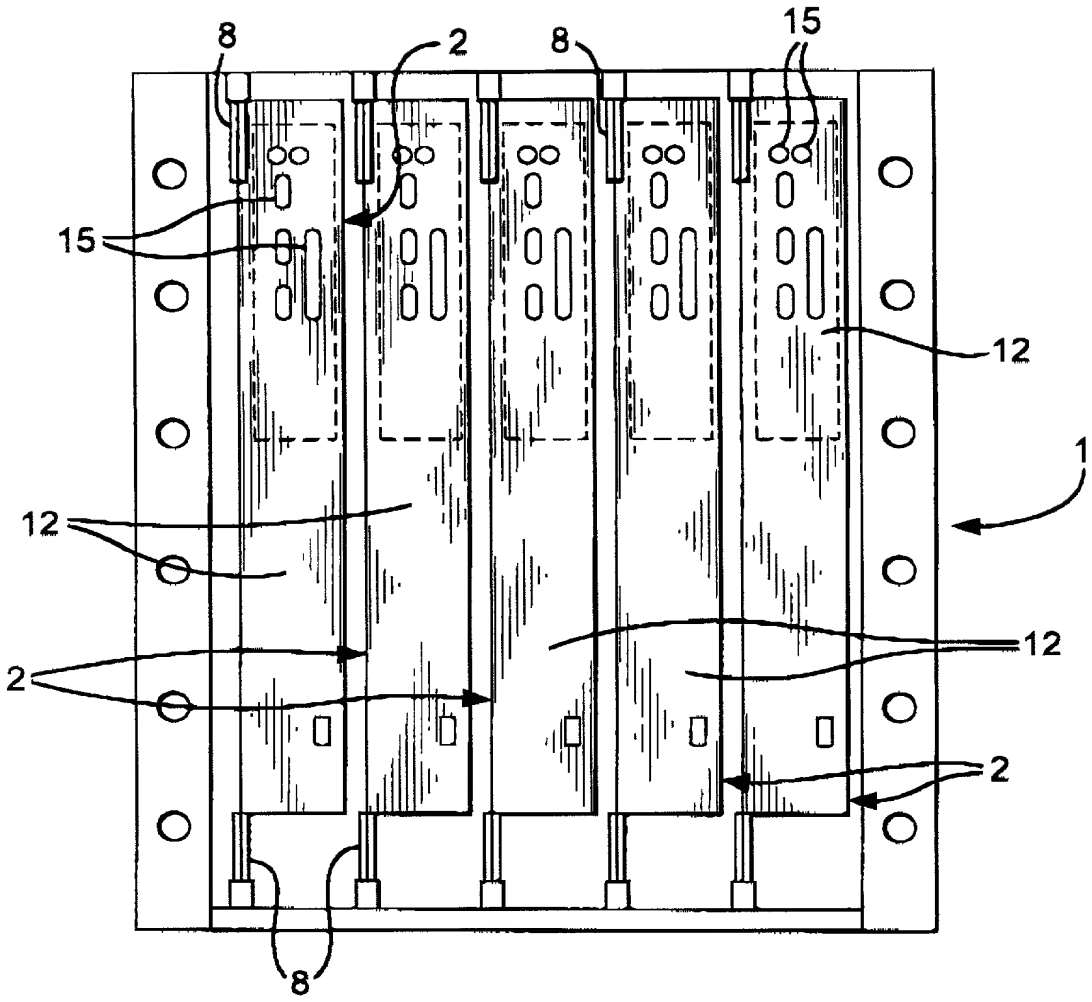

Fig. 1

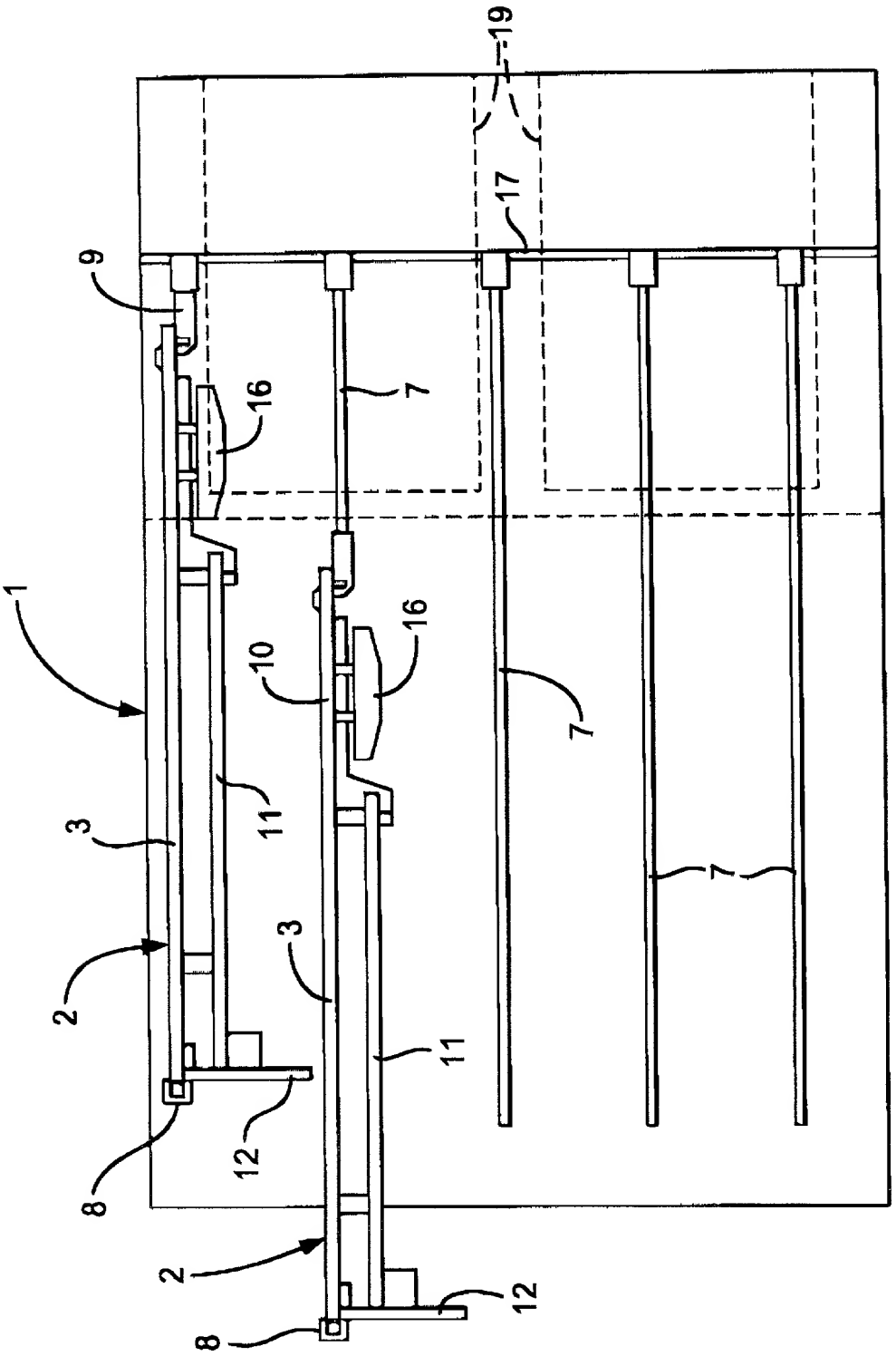

Fig.2

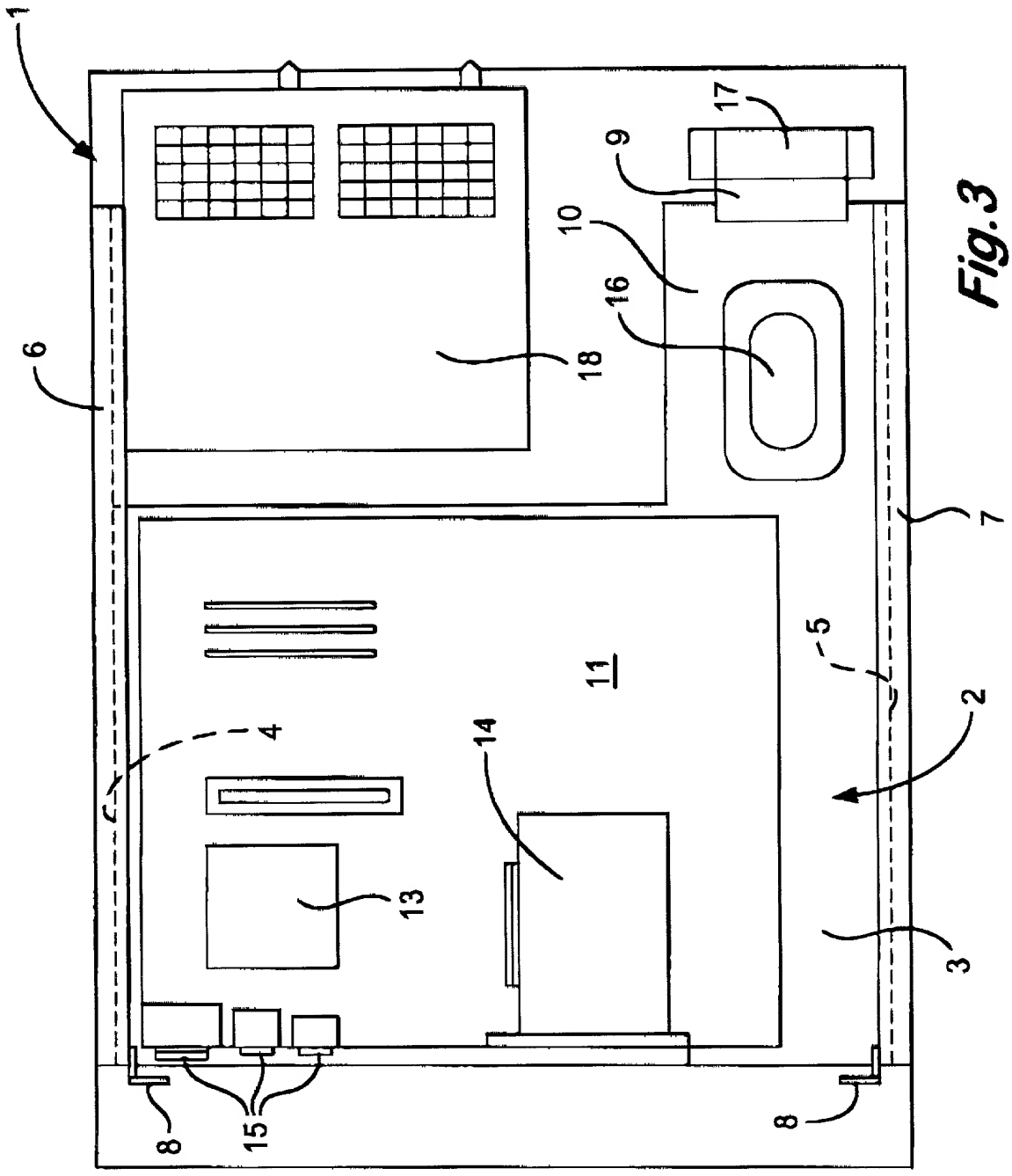

Fig.3

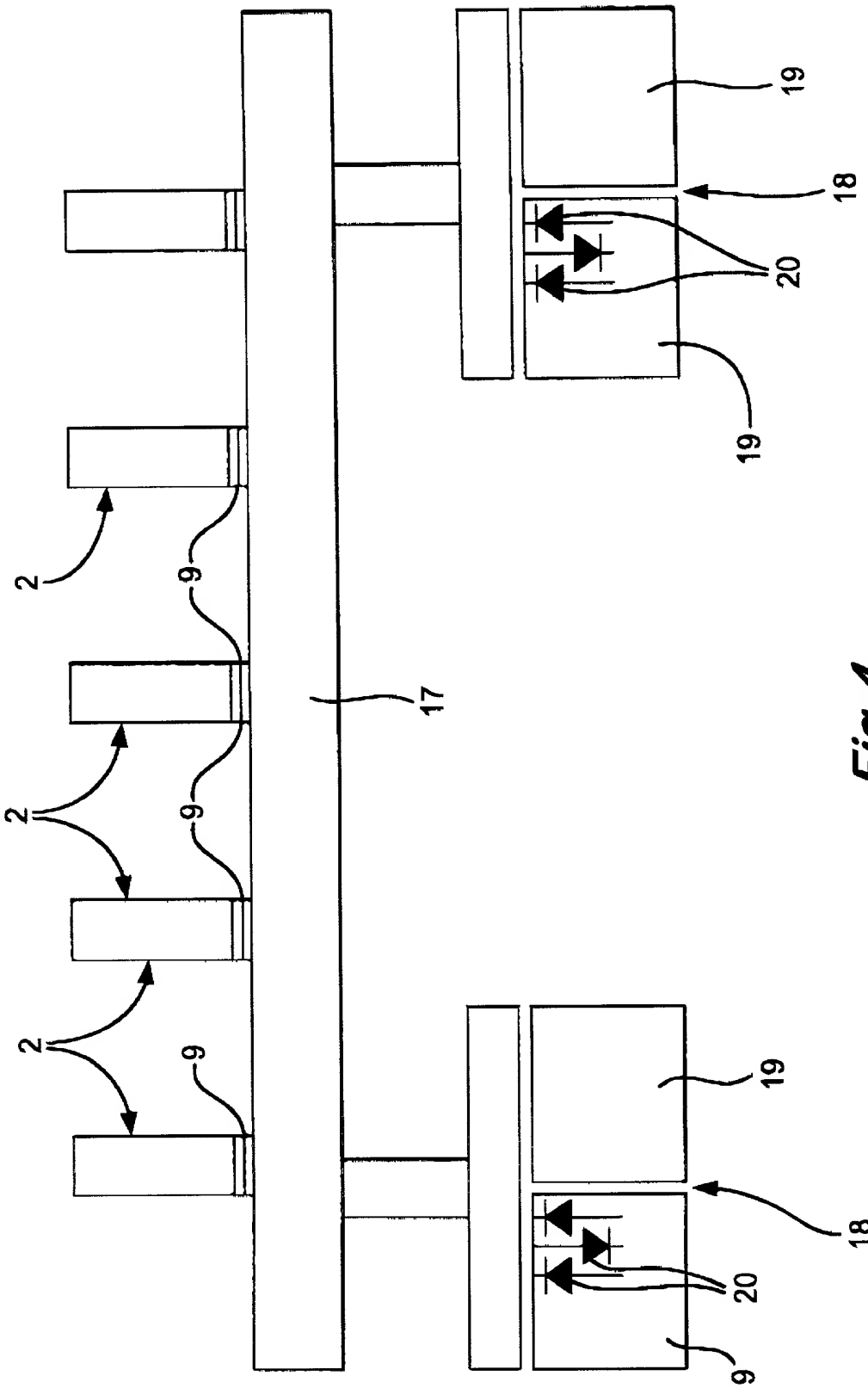

Fig.4

COMBINED DECLARATION AND POWER OF ATTORNEY

(Original, Design, National Stage of PCT, Supplemental)

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is of the following type: (check one applicable item below)

- ■ original
- ☐ design
- ☐ supplemental
- ☐ National Stage of PCT
- ☐ divisional (see added page)
- ☐ continuation (see added page)
- ☐ continuation-in-part (see added page)

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below next to my name. I/We believe that the named inventor or inventors listed below is/are the original and first inventor or inventors of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

COMPUTER SYSTEMS

SPECIFICATION IDENTIFICATION

The specification of which: (complete (a), (b) or (c))

(a) ■ is attached hereto.

(b) ☐ was filed on _____ as
☐ Serial No. _____ or
☐ Express Mail No. _____ as Serial No. (not yet known) and was amended on _____(if applicable).

(c) ☐ was described and claimed in PCT International Application No. _____ filed on _____ _____ and as amended under PCT Article 19 on _____ (if any).

POWER OF ATTORNEY

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name(s) and registration number(s))

Anthony G. M. Davis	Registration No. 27,868
Michael J. Bujold	Registration No. 32,018
Scott A. Daniels	Registration No. 42,462

☐ Attached as part of this Declaration and Power of Attorney is the authorization of the above-named attorney(s) to accept and follow instructions from my representative(s).

Send Correspondence to

Davis and Bujold
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Manchester, NH 03101

Direct Telephone Calls to:

(603) 624-9220

Direct Telefaxes to:

(603) 624-9229

ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent Office all information which is known to be material to patentability of this application as defined in § 1.56 of Title 37 of the Code of Federal Regulations.

PRIORITY CLAIM

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

EARLIEST FOREIGN APPLICATION(S), IF ANY FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

COUNTRY	APPLICATION NO.	DATE OF FILING (day,month,year)	PRIORITY CLAIMED UNDER 37 USC 119
GB	9926858.3	15 November 1999	■YES ☐NO
			☐YES ☐NO
			☐YES ☐NO
			☐YES ☐NO
			☐YES ☐NO

ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole inventor: Robin HARKER

Inventor's signature _____

Date 14th November 2000 Country of Citizenship: England

Residence: Amersham, Buckinghamshire, England

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Buckinghamshire HP6 6EB, England